I. AMENDMENTS TO THE CLAIMS:

Please cancel claims 3-6 and 15 without prejudice. Kindly amend claims 1, 10 and 16, and add new claim 21 as follows.

The present Listing of Claims replaces all previous listings, or versions, of the claims in the above-captioned application.

LISTING OF CLAIMS:

The present listing of claims replaces all prior listings or versions of claims in the present application.

1. (Currently Amended) An SDIO card development supporting system for development of SDIO cards, the system comprising:

(a) a hardware component comprising:

(i) a platform having an operating system and a memory operably connected to the operating system;

(ii) an SD host board including an SDIO host device; ~~and~~

(iii) a first~~an SD~~ bus operably connecting the operating system of the platform to the SD host board; and

(iv) an SDIO controller reference board equipped with an SDIO port operably connectable to the SDIO host device via a SD bus; and

(b) a software component stored in the memory of the platform, wherein the software component comprises an SDIO test program that runs on the operating system of the platform, wherein the reference board comprises

(i) a substrate;

(ii) an SDIO controller disposed on the substrate and equipped with a plurality of application interfaces;

(iii) a quartz oscillator operably connected to the SDIO controller; and

(iv) a plurality of application interface ports operably connected to the SDIO controller, wherein the SDIO controller further comprises a host interface module that operably connects the SDIO controller to the SD bus when the SDIO port is operably connected to the SDIO host device, and wherein the plurality of application interfaces includes a HS-UART interface and a PCMCIA interface, and the plurality of application interface ports includes a HS-UART connector and a PCMCIA connector, wherein the HS-UART interface is operably connected to the HS-UART connector and the PCMCIA interface is operably connected to the PCMCIA connector.

2. (Original) A system as recited in claim 1, wherein the platform is a computer.

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Original) A system as recited in claim 1, wherein the SDIO test program operates to generate commands, analyze commands, trace commands, and perform debugging for the SD host device.

8. (Original) A system as recited in claim 7, wherein the SDIO test program also operates a language script interpreter in order to describe generated commands, analyzed commands, traced commands, and debugging performed by the SDIO test program.

9. (Original) A system as recited in claim 1, wherein the SDIO test program comprises: a command generator; a command analyzer; a tracer; and a language script interpreter.

10. (Currently Amended) An SDIO controller reference board equipped with an SDIO port operably connectable to an SDIO host device via an SD bus, the reference board comprising:

(a) a substrate;

(b) an SDIO controller disposed on the substrate and having a plurality of application interfaces;

(c) a quartz oscillator operably connected to the SDIO controller; and

(d) a plurality of application interface ports operably connected to the SDIO controller, wherein the plurality of application interfaces includes a HS-UART interface and a PCMCIA interface, and the plurality of application interface ports includes a HS-UART connector and a PCMCIA connector, wherein the HS-UART interface is operably connected to the HS-UART connector and the PCMCIA interface is operably connected to the PCMCIA connector.

11. (Original) An SDIO controller reference board as recited in claim 10, wherein the SDIO controller further comprises a host interface module that operably connects the SDIO controller to the SD bus when the SDIO port is operably connected to the SDIO host device.

12. (Original) An SDIO controller reference board as recited in claim 11, wherein the SDIO controller further comprises a memory interface, and the reference board further comprises one or more memory units operably connected to the memory interface.

13. (Original) An SDIO controller reference board as recited in claim 12, wherein the one or more memory units are selected from the group consisting of an I^2C serial EEPROM unit, a NAND-type flash memory and a NOR-type flash memory.

14. (Original) An SDIO controller reference board as recited in claim 12, wherein each application interface of the SDIO controller is operably connected to a respective one of the plurality of application interface ports.

15. (Cancelled)

16. (Currently Amended) A method of operating an SDIO card development supporting system, wherein the system comprises an SD integrated development environment software program operating on a computer platform and the computer platform comprises a memory storing the software program and a SDIO host device, the method comprising the steps of:

(a) starting the SDIO card development supporting system using the software program and optionally checking a work environment;

(b) launching one or more engines of the software program;

(c) initializing the system using the software program when an SDIO card unit, having an SDIO controller reference board comprising an SDIO controller, is inserted into an SDIO slot of the computer platform so as to operably connect the SDIO controller to the SDIO host device, wherein the SDIO controller reference board comprises

(i) a substrate, wherein the SDIO controller is disposed on the substrate and has a plurality of application interfaces;

(ii) a quartz oscillator operably connected to the SDIO controller; and

(iii) a plurality of application interface ports operably connected to the SDIO controller, wherein the plurality of application interfaces includes a HS-UART interface and a PCMCIA interface, and the plurality of application interface ports includes a HS-UART connector and a PCMCIA connector, wherein the HS-UART interface is operably connected to the HS-UART connector and the PCMCIA interface is operably connected to the PCMCIA connector; and

(d) generating an SDIO command using the software program in order to test the operable connection between the SDIO host device and the SDIO controller.

17. (Original) A method as recited in claim 16, wherein the software program comprises an SDIO initialization engine and an SDIO command process engine, and initializing of the system is performed by the SDIO initialization engine and generating the SDIO command is performed by the SDIO command process engine.

18. (Original) A method as recited in claim 16, further comprising the steps of:

(e) comparing behavior of the SDIO controller of the SDIO card unit to behavior of an ideal SDIO controller stored in memory of the computer platform; and

(f) generating an error signal when a difference between the behavior of the SDIO controller of the SDIO card unit and the behavior of the ideal SDIO controller is detected.

19. (Original) A method as recited in claim 16, wherein the operable connection between the SDIO host device and the SDIO controller is provided by an SD bus of the computer platform, and the method further comprises the steps of:

(e) recording a transaction history of packets supported by the bus; and

(f) parsing and analyzing the transaction history in order to debug the software program when the SDIO card unit is a SDIO controller reference board.

20. (Original) A method as recited in claim 16, wherein the operable connection between the SDIO host device and the SDIO controller is provided by an SD bus of the computer platform, and the method further comprises the steps of:

(e) recording a transaction history of packets supported by the bus; and

(f) parsing and analyzing the transaction history in order to debug the SDIO card unit when the SDIO card unit is an actual SDIO card.

21. (NEW) An SDIO card development supporting system for development of SDIO cards, the system comprising:

(a) a hardware component comprising:

(i) a platform having an operating system and a memory operably connected to the operating system;

(ii) an SD host board including an SDIO host device;

(iii) a first bus operably connecting the operating system of the platform to the SD host board; and

(iv) an SDIO controller reference board equipped with an SDIO port operably connectable to the SDIO host device via an SD bus; and

(b) a software component stored in the memory of the platform, wherein the software component comprises an SDIO test program that runs on the operating system of the platform, wherein the reference board comprises

(i) a substrate;

(ii) an SDIO controller disposed on the substrate and equipped with a plurality

of application interfaces;

(iii) a quartz oscillator operably connected to the SDIO controller; and

(iv) a plurality of application interface ports operably connected to the SDIO controller, wherein the plurality of application interfaces includes a HS-UART interface and a PCMCIA interface, and the plurality of application interface ports includes a HS-UART connector and a PCMCIA connector, wherein the HS-UART interface is operably connected to the HS-UART connector and the PCMCIA interface is operably connected to the PCMCIA connector.